Code No: 154AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year II Semester Examinations, April/May - 2023
DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	Write the characteristics of Digital Integrated Circuits?	[2]
b)	Implement XOR gate using only NAND gates.	[3]
c)	Implement a 4×1 mux using 2×1 mux's.	[2]
d)	Simplify the following function in POS form. $F(A, B, C, D) = \sum m(2, 3, 4, 5, 6, 7, 9, 11, 12, 13$	[3]
e)	List the applications of shift registers.	[2]
f)	What are the differences between combinational and sequential logic circuits?	[3]
g)	List the example of A/D converter ICs.	[2]
h)	What is the quantization and encoding process in an ADC?	[3]
i)	What do you mean by sequential memory?	[2]
j)	Write short notes on CPLDs.	[3]

PART – B

(50 Marks)

2.a) In a new number system, X and Y are successive digits such that $(XY)_r = (25)_{10}$ and $(YX)_r = (31)_{10}$. Find X, Y, r.

b) Convert decimal +49 and +29 to binary, using the signed 2's complement representation and enough digits to accommodate the numbers. Then perform the binary equivalent of (+29)+(-49), (-29)+(+49), (-29)+(-49). Convert the answers back to decimal and verify that they are correct. [5+5]

OR

3. Explain the operation of TTL gate with totem pole output configuration. [10]

4.a) Implement the following Boolean expression using 3 to 8 decoder.

$$f(x, y, z) = x' + yz'$$

b) Explain a 4 bit binary adder-subtractor in detail. [5+5]

OR

5.a) i) Find the complement of f = (bc' + a'd)(ab' + cd').
ii) Simplify the following Boolean expression to a minimum number of literals:
f= (x'y'+z)'+z+xy+wz.

b) Design a 4 input priority encoder. [5+5]

6.a) Explain the operation of clocked SR Flip flop with its characteristic table.
b) Design a 3-bit synchronous binary down counter using JK flip-flops. [5+5]

OR

7.a) Explain the operation of 4-bit bidirectional shift register.
b) Show that a Johnson counter with *n* flip-flops produces a sequence of 2 *n* states. List the 10 states produced with five flip-flops and the Boolean terms of each of the 10 AND gate outputs. [5+5]

8.a) What are the specifications of digital to analog converters? Explain.
b) Explain the operation of successive approximation analog to digital converter. [4+6]

OR

9.a) Discuss the operation of binary weighted resistor digital to analog converter.
b) Draw and explain the operation of counter type analog to digital converter. [5+5]

10.a) Explain the operation of 16-bit ROM array with neat diagram.
b) Explain the operation of charge coupled device memory in detail. [5+5]

OR

11.a) Explain the operation of a six transistor CMOS SRAM cell.
b) Implement the following Boolean functions using PLA.
F1 = ∑m(3,5,7)
F2 = ∑m(4,5,7). [5+5]

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